Dear EEE Alumni

Broadcom is recruiting for the position stated below. If you are interested, please write to Mr Tan Cheng Huat at cheng-huat.tan@broadcom.com. Thanks.

Regards
E^3 Alumni
http://www.eee.ntu.edu.sg/alumni

Position for R&D Engineer

Job Description:

1. R&D engineer position available in for physical or DFT implementation of high performance System-On-Chip ASICs. Candidate with one or more of the following key competencies (multiple competencies will be advantageous):
    a. Working experience in physical design implementation of large ASICs (100 to 400 million gates complexity).
    b. Good knowledge of digital logic design with high level description language for highspeed low power design
    c. Knowledge of DFT implementation of ATPG Scan, JTAG, MBIST, Logic BIST, simulation playback, ATPG pattern generation and verification.
    d. Demonstrated ability in providing technical support to customers, 1st proto bring up and failure analysis.
    e. Manage customer working relationship and willingness to travel to support customer system debug.
    f. Demonstrated strong technical hands-on competency in using leading edge physical design EDA tools in projects.
2. Utilize commercial and in-house EDA tools for the design and implementation of 100 ~ 400 million gate integrated circuits in 16nm/7nm/5nm process technologies.
3. Opportunity to participate in innovation, design flow and methodology development to address challenges of designing into deep submicron processes and state-of-the-art ASIC design for computing and networking products.

Qualifications: Requirements

1. Degree, Masters or PhD in Electrical/Electronics/Computer engineering with 5 years or more experience in a relevant field.
2. Familiarity with one or more VLSI design tools for Place&Route, verilog simulation, DRC/LVS verification, timing analysis, HDL design language and scripting languages (perl/Tcl/python).
3. Proficiency in UNIX/Linux is advantageous.