Engineering Assistant and Fresh Graduate Verification IC DESIGN ENGINEERS

Job Description:
Be part of a team in creating state-of-the-art Secure Low Power SoC ARM-based IC/SoC for the wired and wireless connectivity market in a Product Line environment

Responsibilities:
- Capable of using OVM, VMM / UVM test suite for the verification of SoC ARM system with many digital IPs and other communication interfaces.
- To assist in designing of Verification IP from standard industrial specification.
- To implement test cases from product and standard industrial specification to ensure SoC achieve highest possible coverage, using both constraint random and directed test with UPF/CPF and any other formal verification methodology from Synopsys / Cadence.
- To document, compile and correlate all test cases to meet all features in Functional Requirement specification.

Requirements:
- Requires BSc in Electrical and Electronic or Computer Engineering.
- Requires 1 years or more of experience in building UVM/OVM/VMM equivalent test suite is an added advantage.
- Requires good understanding of state of the art verification techniques including assertion and metric-driven verification methodology.
- Basic knowledge of System Verilog, System C, C++, and Verilog.
- Strong experience in working in Synopsys VCS or Cadence IES, and other formal verification tools.
- Able to work in a team with a strong drive to excel.
- Able to work independently on a given assignment and work hard to finish on time.
- Good written and communication skills.

Company Name and Information: Nations Technologies Inc.
https://www.nationstech.com/en/gongsixinxi5/

Interested candidates, please submit your resume to **Singapore_HR@nationstech.com**