EE6601 ADVANCED WAFER PROCESSING

Acad Unit: 3
Pre-requisite: NIL
Effective: AY2014-2015 Semester 2
Last update: 10 October 2013

OBJECTIVE

1. To study deep sub-micron front end process technology
2. To study deep sub-micron back end process technology
3. To study characterization techniques relevant to deep sub-micron process technology

LEARNING OUTCOME

The students will be exposed to state-of-the-art advanced CMOS process technologies. They will also be exposed to future technology. They will also become more familiar with the relevant diagnostic techniques for process related issues.

OTHER RELEVANT INFORMATION

Prior knowledge required: some basic knowledge of MOSFETs and CMOS technology
Level of difficulty: medium
Mathematics: simple

CONTENT

Dielectrics for CMOS technology. Chemical and mechanical polishing. Lithography and resist technology. Etching process and technology. Backend interconnect technology. Cleaning technology. Process integration. Metrology and analytical techniques

ASSESSMENT SCHEME

Continuous Assessment: 20%
Final Examination: 80%

TEXTBOOKS

1. James D. Plummer, Michael D. Deal, and Peter B. Griffin "Silicon VLSI Technology: Fundamentals, Practice, and Modeling," ISBN-13: 9780130850379, Prentice Hall, 2001.
2. C. Y. Chang and S. M. Sze, "ULSI Technology," ISBN 9780071141055, 1996.

REFERENCES

1. Gang He and Zhaoqi Sun (eds.), "High-k Gate Dielectrics for CMOS Technology", ISBN 978-3-527-33032-4 - Wiley-VCH, Weinheim, 2012
2. Karen Reinhardt and Werner Kern (Editors), "Handbook of Silicon Wafer Cleaning Technology", 2nd Edition, ISBN-13**:** 978-0815515548, William Andrew, 2008
3. David G. Seiler, Alain C. Diebold, T. J. Shaffner, Robert McDonald, Stefan Zollner (editors), "Characterization and Metrology for ULSI Technology 2003: International Conference on Characterization and Metrology for ULSI Technology, Austin, Texas 24-28 March 2003", *Volume 683 of AIP CONFERENCE PROCEEDINGS*, ISBN 0735401527, 9780735401525, American Institute of Physics, 2003