NM6604 Laboratory 1: Semiconductor Process and Device Simulation

Process models: diffusion, oxidation, implantation. Process variables/targets: doping profiles, junction depths, oxide thickness. Process simulation: Simulate a given sub-micron CMOS process recipe and study profiles and layer structures. Physical models. Numerical algorithms and solutions. Device performance parameters. Short-channel effects. DC simulations. Device simulation: Simulate the DC characteristics of the “fabricated” device and analyze device operation with respect to potential, field, and carrier distributions as well as terminal I–V characteristics. Wafer-split experiment. Device-target vs. process-variable relations. Transistor performance optimization/trade-offs through process variation. Technology development and optimization. Design of Experiment (DOE): Implement a computer experiment to study the scaling characteristics (varying gate length) of the given sub-micron technology. Study the influence of process variations on device performance parameters.